REMARKS

I. Status of the Application

Claims 37-60 are pending in this application. In the September 24, 2003 office action, the Examiner:

1. Rejected claims 37-44, 50, 52-54 and 60 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. U.S. 5,619,142 to Schweer et al. ("Schweer");

2. Rejected claim 51 under 35 U.S.C. § 103(a) as allegedly being obvious over Schweer in view of Horowitz & Hill, The Art of Electronics (Cambridge University Press, 1989)("Horowitz and Hill"); and

3. Deemed claims 20-24 allowable if rewritten to incorporate all of the limitations of the base claim and any intervening claim.

In this response, applicant has amended claims 37, 40, 53, 54, and 60 to clarify the inventions claimed therein. Applicant gratefully acknowledges the allowance of claims 55-59, as well as the allowability of claims 45-49. Applicant requests reconsideration and allowance of the claims 37-44, 50-54 and 60 in view of the foregoing amendments and the following remarks.

II. Claims 37-40 are Not Anticipated

Claims 37-40 stand rejected as allegedly being anticipated by Schweer. However, for reasons discussed below in detail, Schweer fails to teach or suggest each and every element of any of claims 37-40.

A. Claim 37

Claim 37, as amended, is directed to an arrangement for use in an electricity meter that is coupled to an external transformer to measure electricity consumption on a power line. The arrangement is operable to compensate for measurement errors and includes a source of digital measurement signals, a memory, and a processing circuit. The source of digital measurement signals includes an internal sensor circuit and an analog-to-digital conversion circuit. The internal sensor circuit is operable to receive power line signals from the external transformer and generate measurement signals therefrom. The analog-to-digital conversion circuit is operable to convert the generated measurements signals to digital measurement signals.

The memory stores data representative of at least one error rating for the external transformer. The processing circuit is operably coupled to the source of digital measurement signals to receive the digital measurement signals therefrom. The processing circuit is operable to obtain at least one electricity consumption measurement value corresponding to at least a part of the digital measurement signals. The processing circuit is also operable to adjust the at least one electricity consumption measurement value using at least a portion of the stored data.

Claim 37 thus recites, among other things, an internal sensor circuit that generates measurement signals that are converted to the digital measurement signals by the analog-to-digital conversion circuit.

1. Amendments Do Not Constitute New Matter

The amendments to claim 37, which relate to the analog-to-digital conversion circuit and the internal sensor circuit, are fully supported by the specification as originally filed and therefore do not constitute new matter. By way of example, support for the amendments may be found in the original application at page 12, lines 7-17.

B. Schweer

Schweer has formed the basis for the prior art rejections in all prior office actions, and therefore will not be discussed in detail. However, it is noted that the Examiner has cited the zero crossing detector 66 of Schweer as constituting the claimed *internal sensor circuit.* As amended, however, claim 37 clarifies that the internal sensor circuit is operable to generate measurement signals that are converted to digital measurement signal by the analog-to-digital conversion circuit.

C. Schweer Does Not Teach an Internal Sensor Circuit as Claimed

The zero crossing detector 66 of Schweer does not generate measurement signals from the power line signals as claimed. The zero crossing detector 66 merely generates a *timing* signal used by the A/D converter of Schweer. Instead, the measurement signals are generated in Schweer by the CTs 10, the PT 60 and the shunts 10b.

In particular, the discussion regarding the zero crossing detector 66 may be found at col. 5, line 66 to col. 6, line 17. In pertinent part, the discussion states:

> The zero crossing detector 66 communicates with the A/D converter 62 and the processor 70 along a path 74 to initiate signal conversion on the bus 64 when a zero crossing is detected in the voltage waveform.

(Schweer at col. 6, lines 14-17; see also Fig. 8). Thus, the zero crossing detector 66 only

provides a signal indicating *when* signal conversion is to be initiated. The zero crossing signal is *not* a measurement signal and is *not converted* by the A/D converter 62. Instead, the zero crossing signal is merely a timing signal. (See also *id.* at col. 7, lines 10-55).

As shown in Fig. 8, the measurement signals that are converted in Schweer are those generated by the CTs 10, the PT 60 and the shunts 10b. Those elements may either constitute external transformers, or internal sensors, but cannot constitute both. Moreover, the Examiner has not alleged that any of those elements constitutes an internal sensor circuit.

As a result, Schweer fails to teach, show or suggest an "internal sensor circuit configured to convert power line signals received from the external transformer to measurement signals, [and an] analog-to-digital conversion circuit configured to receive the measurement signals from the sensor circuit and convert the measurement signals to digital measurement signals" as called for in claim 1 as amended. For this reason, it is respectfully submitted that the anticipation rejection of claim 1 is in error and should be withdrawn.

D. Claims 38-40

Claims 38-40 also stand rejected as allegedly being anticipated by Schweer. Claims 38-40 all depend from and incorporate all of the limitations of claim 37. Accordingly, for at least the same reasons as those set forth above in connection with claim 37, it is respectfully submitted that the rejection of claims 38-40 should be withdrawn.

1. Additional Independent Grounds for Patentability of Claim 40

In addition, claim 40 is patentable for reasons independent of those discussed above in connection with claim 37. In particular, claim 40 recites that the processing circuit is also "operable to adjust the . . . electricity consumption measurement value using an internal calibration value, the internal calibration value *corresponding to at least one error* associated with the internal sensor circuit". Accordingly, the processing circuit of claim 40 is operable to adjust for errors due to both internal sensors *and* external transformers. Schweer teaches no such processing circuit. In particular, even if it were assumed that the zero crossing detector 66 constituted the claimed internal sensor circuit, which it does not, Schweer does not teach a processing circuit or any other device that adjusts *anything* corresponding to an error of that zero crossing detector. Indeed, Schweer does not acknowledge the presence of any error caused by the zero crossing detector 66. At best, the zero crossing detector 66 plays a role in correcting errors in the external transformers. (See *id.* at col. 7, lines 3-10).

Accordingly, in addition to the reasons discussed above in connection with claim 37, the rejection of claim 40 should be withdrawn for independent reasons.

III. Claim 41

Claim 41 stands rejected over Schweer. In the applicants' Response to Office Action and Rule 114 Submission dated September 1, 2004, plain arguments were set out regarding the patentability of claim 41. These arguments stated basically that claim 41 recites a processing circuit that adjusts a value that is representative of a *waveform sample*. A waveform sample as that term is known in the art, and which is consistent

with the disclosure, is an instantaneous value of a waveform. (See application, elements 42 of Fig. 2). By contrast, Schweer only teaches the adjustment of an RMS voltage and/or current RMS. An RMS voltage value is not an instantaneous value of a waveform, but rather is a statistical value derived from several samples. An RMS voltage value may be derived from several waveform samples, but is not itself representative of a single waveform sample. Thus, Schweer does not teach a processing circuit operable to adjust an electricity consumption measurement value, wherein that value is representative of a "waveform sample".

In the "Response to Arguments" of the most recent office action, the Examiner deemed this argument not persuasive. (September 24, 2004 office action at p. 8). In particular, the Examiner contended: "[Applicant argues that] Schweer does not correct sampled data; however, this is shown at column 9, line 15 to column 10, line 15". (Id.)

It is respectfully submitted that columns 9 and 10 does not show the correction of a value that is representative of a waveform sample. Columns 9 and 10 show the correction of RMS values and phase error value. However, it is unclear what the Examiner is alleging. Is the Examiner stating that column 9 and 10 teach adjustment of something *other* than RMS voltages and currents, or is the Examiner alleging that the adjustment of an RMS value *constitutes* the adjustment of a value representative of a waveform sample?

Regardless, it is clear that an RMS value is not representative of a waveform sample, but rather representative of a sum of squares of a large amount of waveform samples. It is also clear that columns 9 and 10 of Schweer teach adjustment of only RMS values, not individual waveform sample values.

For the foregoing reason, claim 41 is allowable over Schweer.

IV. Claims 42-44, 50-54 and 60

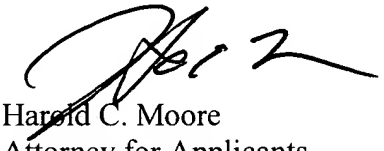
Claims 42-44, 50, 52-54 and 60 also stand rejected as allegedly being anticipated by Schweer. Claim 51 stands rejected as allegedly being obvious over Schweer and other prior art. Claims 42-44, 50-54 and 60 all depend from and incorporate all of the limitations of claim 41, and all rely on the reasoning applied to the rejection of claim 41. As discussed above, the rejection of claim 41 over Schweer is in error and should be withdrawn. Accordingly, for at least the same reasons as those set forth above in connection with claim 41, it is respectfully submitted that the rejection of claims 42-44, 50-54 and 60 should be withdrawn.

In addition, claim 54 is also patentable over Schweer for reasons similar to those discussed above in connection with claim 37. Claim 60 is also patentable over Schweer for reasons similar to those discussed above in connection with claim 40.

V. Conclusion

For all of the foregoing reasons, it is respectfully submitted that the application is in a condition for allowance. Favorable reconsideration and allowance of this application is, therefore, earnestly solicited.

Respectfully Submitted,



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